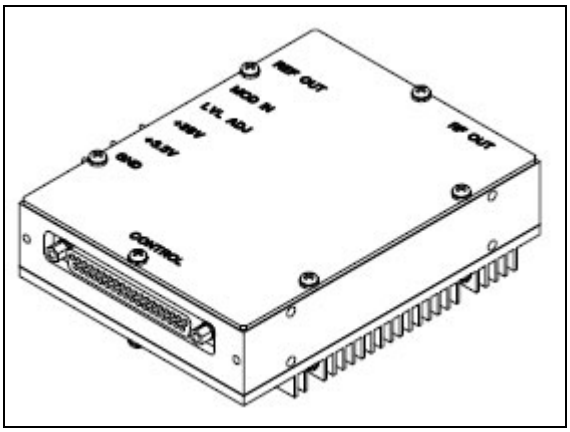
Sintec Optronics

AOM Driver (RF Driver) 64020-200-2ADMDFS-A



A digital frequency synthesizer OEM module with analog and digital modulation input and a 2 Watt RF output. When specified as R64020-200-2ADMDFS-A, the unit delivered will be manufactured to be compliant with EU Directive 2002/95/EC for reduction of hazardous substance.

PARAMETER	SPECIFICATION
Bandwidth:	20 – 200 MHz typical
Clock Frequency:	1000 MHz
Step Size:	< 1 Hz with 30 Bits input
Frequency Settling Time:	250 ns Maximum
Power Out:	2 watts typical
Harmonic Distortion:	2nd:-20 dBc Maximum; 3rd: -15 dBc Maximum
Analog Modulation:	0 to +1 volt Analog into 50 ohm, +1volt = Full RF power output.
Digital Modulation:	1) TTL levels; 2) TTL Active High = Full RF output power; 3) TTL Active Low = Minimum RF output power; 4) No Signal = Full RF output power (pulled high internally)
Rise and Fall Time:	20 ns
Extinction Ratio: Digital:	30 dB Minimum
Analog:	40 dB Minimum
Reference Out:	A reference signal from the un-modulated output of the synthesizer. +0 dBm nominal
Applied Power:	+ 28 volts DC @ 1 amp Maximum + 3.3 volts DC @ 1 amp Maximum
MAXIMUM RATINGS:	
Ambient Temperature:	400 C
RF Output:	No DC Feedback
Supply Voltage:	30 volts DC; 3.5 volts DC
INPUT / OUTPUT CONNECTIONS:	
+28v, +3.3V, and Gnd	Filtered Feedthru
Mod In	SMC Male
Reference Out	SMC Male
RF Output	SMA Female
"FREQUENCY SELECT" Control	TTL 30 bit binary word, Digital Modulation Input, Reset, and a Latch control input through the 37 pin D sub connector.
Dimension	140x109x40.6mm
Outline Drawing	53D3887

CONTROL WORD CALCULATIONS

The output frequency and step size is a function of the clock rate and the "FREQUENCY SELECT" data. The output frequency can be calculated from the formula:

$$f_{out} = \frac{(f_c)(k_{10})}{2^n}$$

Where: f_c = clock frequency in Hz
k_{10} = input word in decimal notation
n = 31 *See note below.

The minimum output frequency and step size are given by:

$$f_{min} = \frac{f_c}{2^n}$$

An example of setting the frequency:
Clock frequency = 1000×10^6 Hz
Desired output frequency = 30.00×10^6 Hz

$$K_{10} = \frac{f_{OUT\,(Hz)}(2^{31})}{f_{OSC\,(Hz)}}$$

$$K_{10} = \frac{30 \times 10^6 (2^{31})}{(1000 \times 10^6)}$$

$K_{10} = 64424509.44$ Decimal

Convert K_{10} to HEX \/- MSB \/ - LSB

K_{HEX} = 3D70A3D → 03D70A3D -Setting for front panel "HEX" switches
NOTE: The switches on the front panel of the driver are LSB to MSB - right to left.

Convert K_{HEX} to Binary \/ LSB - pin1

K_B = 0000111101011100001010001111101 -Setting for binary word input to back panel "FREQUENCY SELECT" 37 pin D-sub connector
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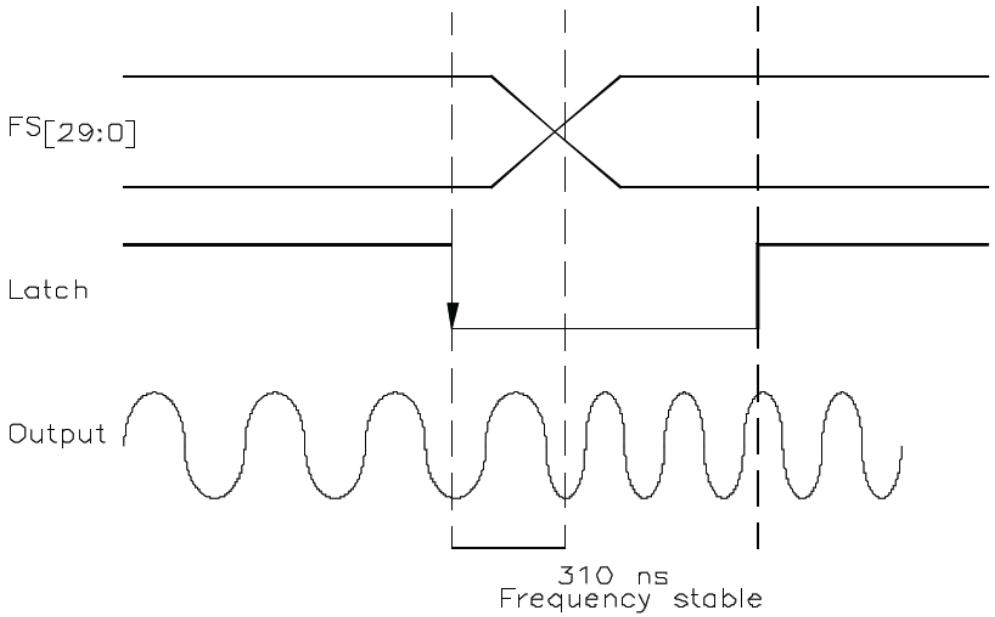
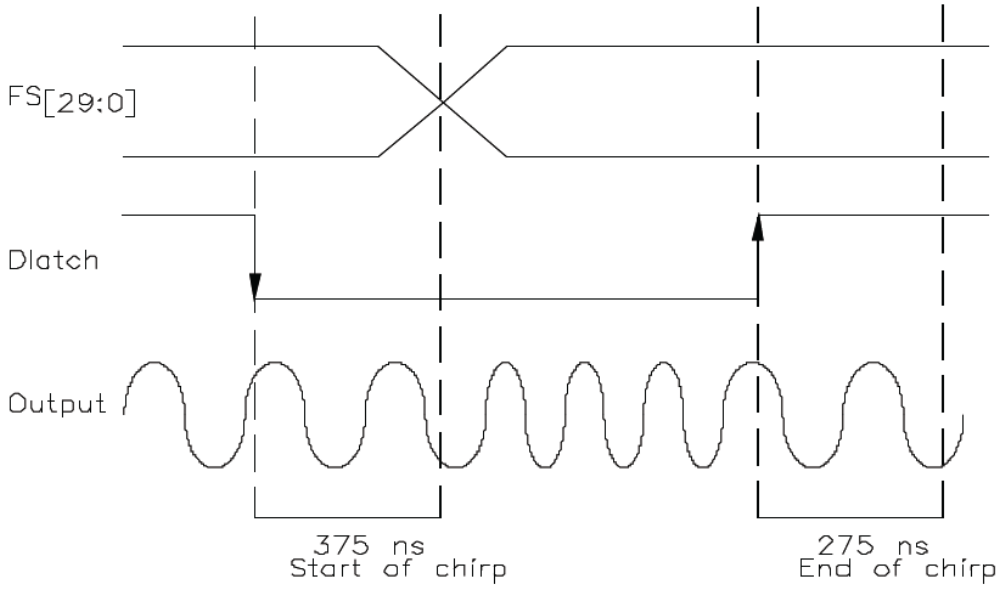
These 4 bits are added to complete the 30 bit word

*Note: (1) This system only uses 30 bits to set the frequency output from the driver. The accumulator inside the chip is 31 bit, so use 231 in your calculations for precision. (2) The LATCH function (pin 16) is a TTL compatible input which is used to load new frequency information into the driver. Frequency data is loaded into the driver when the signal on the LATCH pin goes from HIGH to LOW (falling edge). (3) Master RESET is a TTL active HIGH and resets the accumulator to zero, ie, no frequency output, when a TTL HIGH is applied to pin 17. This is pulled LOW via. a 1 KΩ resistor.

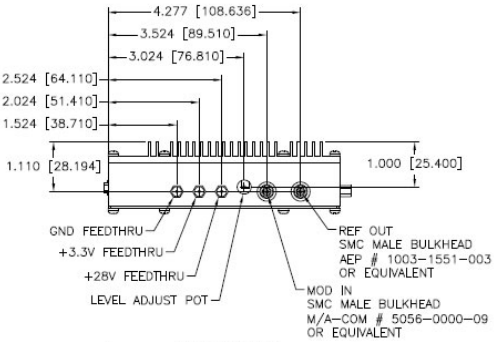
To generate a single frequency, apply the binary frequency word to the FS input, A falling edge on the LATCH input will then load the data and change the frequency.

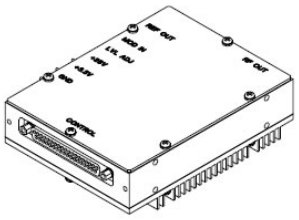


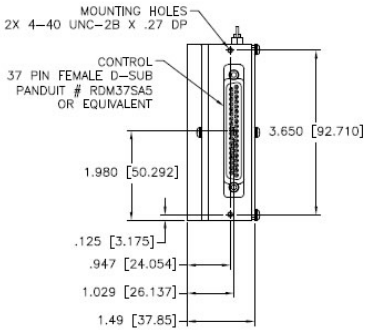
To generate a ferquency chirp, set the starting frequency as above and then apply the delta word to the FS input. A falling edge on DLATCH will then load the delta frequency word and initiate the chrip. The chirp will stop and output will return to to starting value or a rising edge.

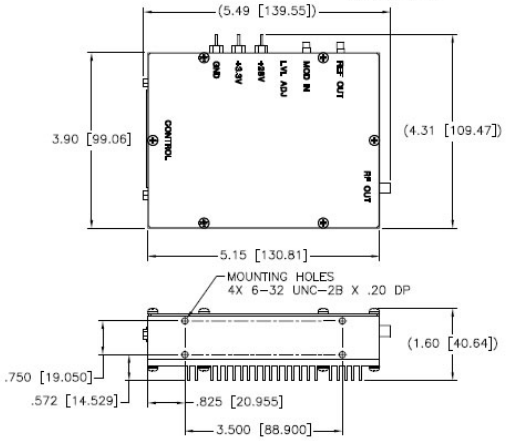


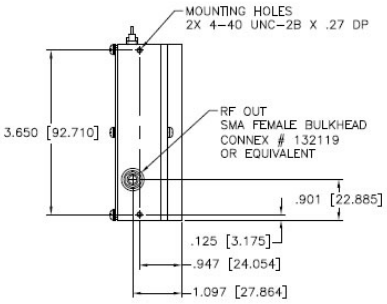
NOTES: UNLESS OTHERWISE SPECIFIED
1. DRAWING PREPARED IN ACCORDANCE WITH MIL–STD–100.
2. INTERPRET 3RD ANGLE PROJECTION. (ISO–A).
3. DIMENSIONING AND SYMBOLS PER ASME Y14.5M–1994.











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